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The Ferroelectric Memory and its Applications

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Abstract. The ferroelectric memory is not only an ideal memory with clear advantages such as non-volatility, low power consumption, high endurance and high speed writing, but is also the most suitable device for memory embedded applications. Its manufacturing process makes it more compatible with the standard CMOS process than the traditional non-volatile memory process, since it does not require high voltage operation, and the ferroelectric process does not influence the characteristics of the CMOS devices used in logic cells, analog cells and core cells. In the spreading of Intellectual Property (IP) application for the LSI Industry, this embedded application takes on a more important role.

In the near future, the ferroelectric memory technology will be taken into reconfigurable devices as programmable interconnect switches besides being used as embedded memories. These ferroelectric memory based reconfigurable devices can be used as Dynamic Programmable Gate Array (DPGA), which are able to be reconfigured from their original logic in a system under an operation mode.

New logic circuits will operated with lower power consumption or a resume function by introducing ferroelectric gated transistors or ferroelectric capacitors.

Even though ferroelectric memory technology has many advantages, it is not popular yet, since, the conventional semiconductor process degrades the ferroelectric layer easily. The means to prevent degradation of ferroelectric films in the silicon wafer process will also be discussed.

Introduction

The needs for lower power and non-volatility in memory devices are increasing by the magnifying demand for portable electronic apparatuses such as mobile phones.

PDA requires not only higher speed access but also higher speed writing. The conventional non-volatile memories have limited endurance up to 1 million cycles, which is not enough for the variety of applications using non-volatile memories.

Battery back up SRAMs should be replaced by non-volatile memories from the viewpoint of the ecology problems.

The development work of ferroelectric memories has been around since the 1960s [1], but the technology has not spread as fast as other silicon technology, because the introduction of a new material such as PZT ($PbZr_xTi_{1-x}O_3$) to the silicon process is not welcome.

In 1988, a 1T1C (1 transistor and 1 capacitor) nonvolatile ferroelectric memory [2] was presented, and demonstrated the potential to be a practical memory. The further progress of thin film technology of PZT and $BiSr_2Ta_2O_9$, and strong demands on nonvolatile memories for portable system applications have been promoting the development of ferroelectric memories.

Today serial 4k–64k FRAMs and FRAM embedded RF-ID chips are available at the market.

Features of Ferroelectric Memories

Conventional non-volatile memories are ROM type only, and are used in limited application areas. On the other hand, ferroelectric memories are non-volatile RAM, and will provide a wider field of application than existing conventional memories.

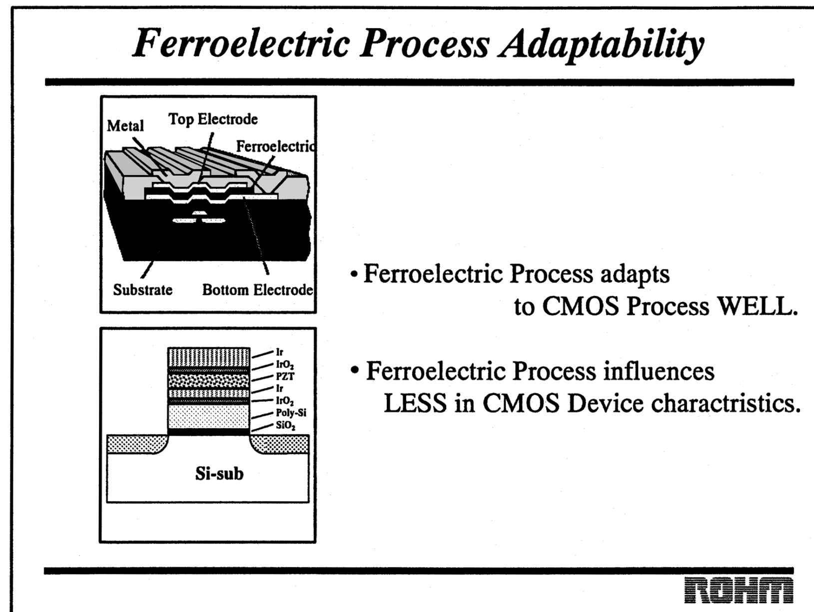

Fig. 1. Ferroelectric process adaptability.

There are 2 types of memory operation principals for ferroelectric memories as shown in Fig. 1. One type is detecting the charge of stored electric charges (the differential between the polarization switching charge current and the polarization non-switching charge current), another type is detecting the difference of the FET channel conductance. This channel conductance is modified by the polarization direction of the ferroelectric film on the FET channel region. The former type of ferroelectric memories are practically used, the later type enables non destructive read out, but does not exist for practical use yet, only the memory cell operation has been demonstrated [3–4].

The ferroelectric memory has the feature as a non-volatile RAM as shown in Fig. 2. Writing endurance cycles up to 10^{10}–10^{13} cycles have been reached. The recent work on $BiSr_2Ta_2O_9$ [5] ferroelectric material or IrO_2 electrode [6] have improved the fatigue of switching charge amount, and indicate that even more than 10^{12}–10^{13} cycles can be achievable. 100 nsec writing speed of FRAM is almost at the same level as SRAM and DRAM, and is much faster than the writing speed of conventional non-volatile memory.

As FLASH and EEPROM are using F-N tunnel or hot electron for the electron injection or erasing, so that a charge pump to generate high voltage (12–15 V) is required internally even when 2 V external single power supply is applied.

On the other hand, the ferroelectric memory is operated at 3 V now, it will be operated at 1.5 V in the near future. Because 1.5 V saturation on P-E hysteresis curve has been reported [7].

At the present time, the cell size of ferroelectric memories are not small enough $(6.2 \times 5.6\,\mu m^2/\text{cell})$ [8], because the ferroelectric process technology is not well established yet for a half micron level patterning.

But, once fine process technology becomes available, ferroelectric memories will have the potential to achieve a cell size compatible to a DRAM cell size with 1T1C cell in comparison with the same design rule as shown in Fig. 3. When the 1T (1 transistor) cell become available, the size will be close to the cell size of a flash memory.

Process Technology and Device Reliability

Ferroelectric memory technology brings many features to us, even FRAMs and FRAM embedded RF-

Comparison of Memory IC

	Nonvolatile Memory		Read Only Memory				Random Access Memory	
	FFRAM	FRAM	FLASH	EEPROM	EPROM	MaskROM	DRAM	SRAM
Access Time	60ns	200ns	120ns	150ns	120ns	120ns	70ns	70ns
Programing Time	100ns	400ns	10μs	10ms	10ms	N/A	70ns	70ns
Programing Voltage	5V	5V	12V	12.5V	12.5V	N/A	5V	5V
Erase Time	0ns	0ns	10^9ns	0ns	(15Wsec/cm^2)	N/A	0ns	0ns
Endurance	10^{12}	10^{10}	10^4	10^4	10^3	N/A	∞	∞
Retention	10Year	10Year	10Year	10Year	10Year	∞	0	0
Operation Current	1mA	5mA	10mA	80mA	10mA	35mA	70mA	10mA
Standby Current	50μA	200μA	50μA	300μA	1μA	100μA	100μA	2μA
Cell Area	0.8~1	1~2	0.8	1	0.8	0.5	1	3~4
(Condition)	(16MHz)	(5MHz)	(6MHz)	(6MHz)	(1MHz)	(8MHz)	(14MHz)	(14MHz)
Product	Nontitle	FM1208	i28F010	AT28C010	HN27C101AG-12	LH530800A	M5M418125A-7S	HM628128BL-7

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Fig. 2. Comparison of memory IC.

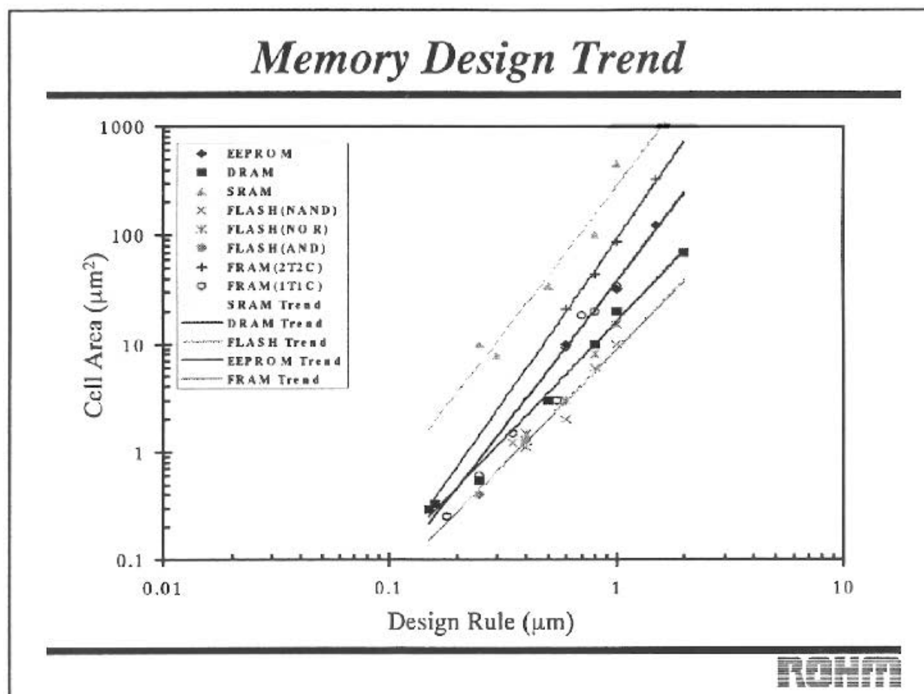

Fig. 3. Memory design trend.

ID chips are available in the market now, but still many of the process technology problems should be solved before making FRAM a universal memory.

The first problem is a fine pattern technology. Ferroelectric films such as PZT and Pt, Ir or IrO_2 electrodes are very difficult to form by anisotropic etching without creating a side wall barrier. The inherent non-volatility of etch products of the materials used in FRAM such as Ir/IrO_2, Pt and PZT forces the abandonment of regular etching processes.

The etching profile of the ferroelectric capacitor is shown on Fig. 4. A 50 degree of slope etch is required to prevent sidewall deposition and to minimize the damage to the PZT film during or after etching of the Ir/IrO_2 top electrode. This slope etch increases the difficulty to minimize the layout rule of the FRAM device. Also, the inherently non-volatile etching materials create many particles in the etching chamber. Future process development for the ferroelectric film etching and electrode films etching is required to proceed to 0.35 μm layout devices.

The second problem is ferroelectric film deposition. In general, sputtering and sol-gel methods have been applied for ferroelectric film formation. The quality of films formed by these methods are not good enough at this time. Further development on other film deposition methods such as MOCVD (metal organic chemical vapor deposition) are strongly required for a higher density memory. The bottom electrode film should also be improved to enable growth of good quality crystals of ferroelectric films on top of it.

The third problem is the retention problem. This problem has become less of an issue by introducing the IrO_2 electrode, especially under high temperature. This problem seems to be related to the second problem, the formation of oxygen vacancies and/or Pb vacancies cause the poor retention problem. The imprint effect of PZT films causes opposite data retention problems occasionally. This problem happens, when one site of data has been kept a long time under a high temperature, and then writing the opposite site of data on the same bit, sometimes the data retention is not long enough. This problem is caused by the decreasing margin between $+Qp^+$ and $-Qu^-$ as shown in Fig. 5. But, this opposite data retention problem is improved, if the opposite site of data is written more than two times on the bit. The

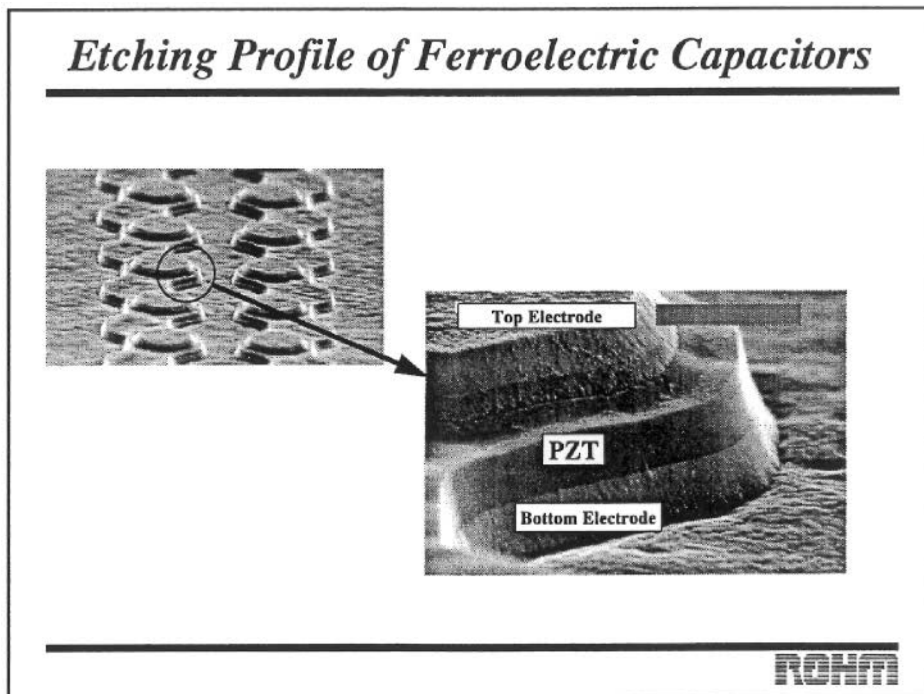

Fig. 4. Etching profile of ferroelectric capacitors.

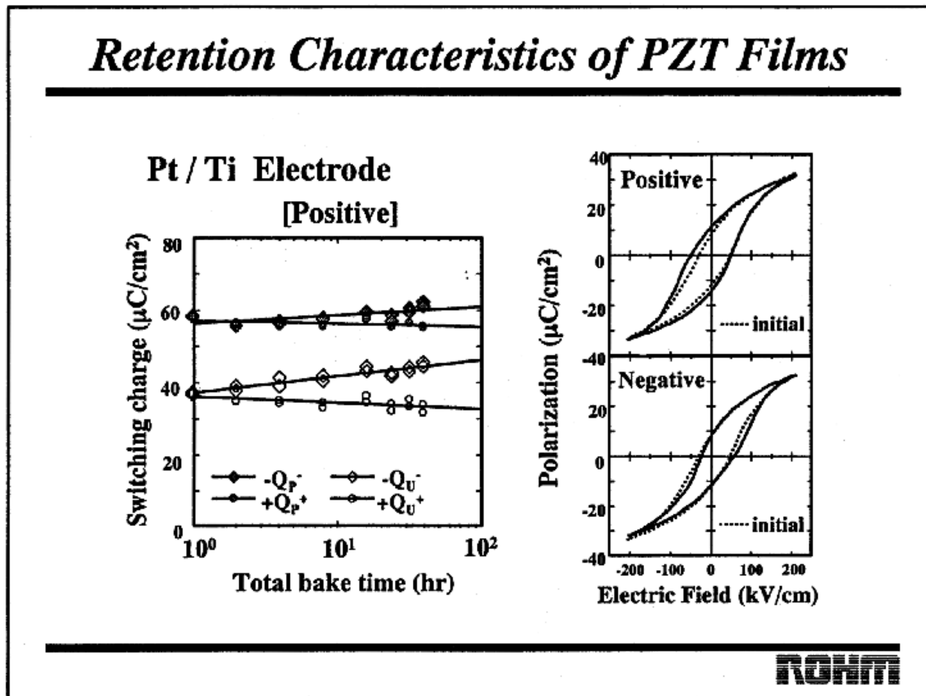

Fig. 5. Retention characteristics of PZT films (Pt/Ti electrode).

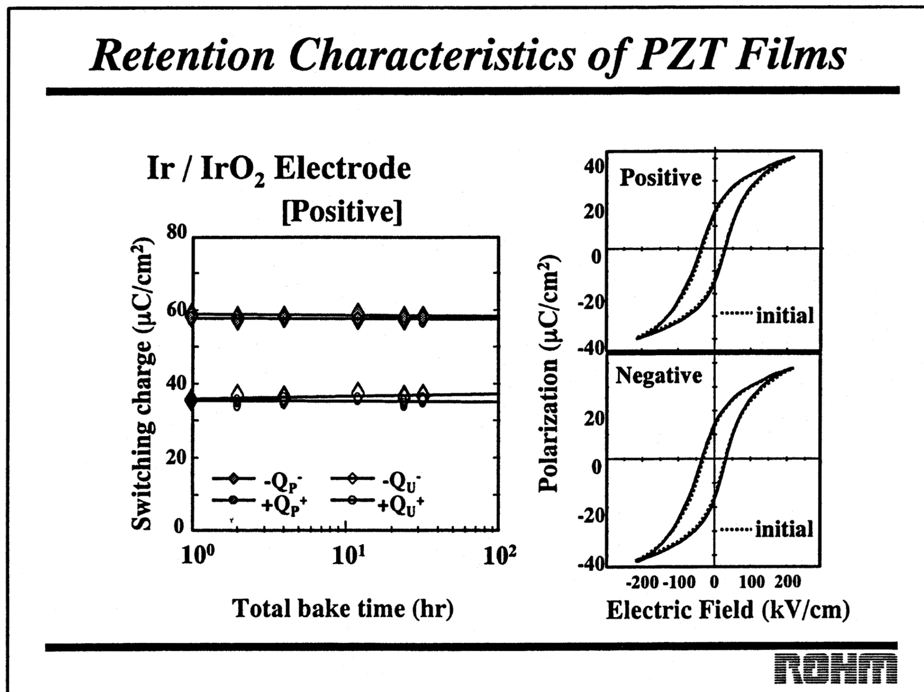

Fig. 6. Retention characteristics of PZT films (Ir/IrO_2 electrode).

recent studies of ferroelectric films such as $BiSr_2Ta_2O_9$ and IrO_2 electrodes show good results on this problem as well as on the fatigue problem of switching charge of a ferroelectric capacitor as shown in Figs. 6 and 7. Hydrogen content atmosphere such as passivation process affects polarization characteristics of Pt/PZT/Pt structured ferroelectric thin film capacitors. The PZT film itself is not degraded when annealed in a hydrogen atmosphere even at 400°C as shown in Fig. 8 [9]. The catalytic effect of platinum for hydrogen reaction enhances this problem [10].

To minimize this hydrogen induced degradation, IrO_2 top electrode ferroelectric capacitors have been studied. As shown on Fig. 9, the electrode induced process degradation on ferroelectric polarization characteristics depends on the top electrode material. IrO_2 top electrode PZT capacitors have reduced hydrogen induced process degradation compare to Pt top electrode PZT capacitors.

The reliability of ferroelectric memory devices is confirmed to be at the same level as regular LSI devices. Several unique tests have been carried out to evaluate the ferroelectric film in addition to regular reliability/life tests of semiconductors, such as fatigue, imprint, retention and etc. The results are shown in Fig. 10.

Process Compatibility

The ferroelectric process takes the place after CMOS device formation, before the contact operating process. The ferroelectric process does not modify the CMOS devices formed under the ferroelectric film, since the process does not have a high temperature treatment, and does not change the source and drain diffusion depth. However, as ferroelectric films are so sensitive to the hydrogen ambient widely used in the semiconductor manufacturing process. A modified process is required to minimize the hydrogen degradation.

Conventional non-volatile memories such as EEPROM and FLASH require high voltage transistors for writing and erasing, and high voltage transistors formation processes change the original CMOS devices, which are, used in the non-high voltage circuit region. From this effect, when EEPROM or

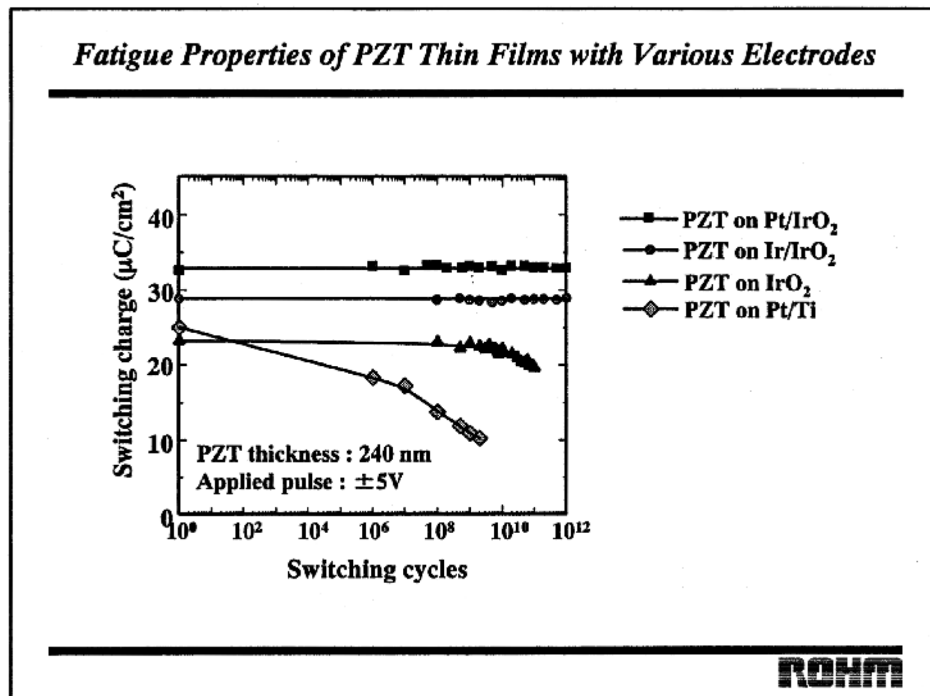

Fig. 7. Fatigue properties of PZT thin films with various electrodes.

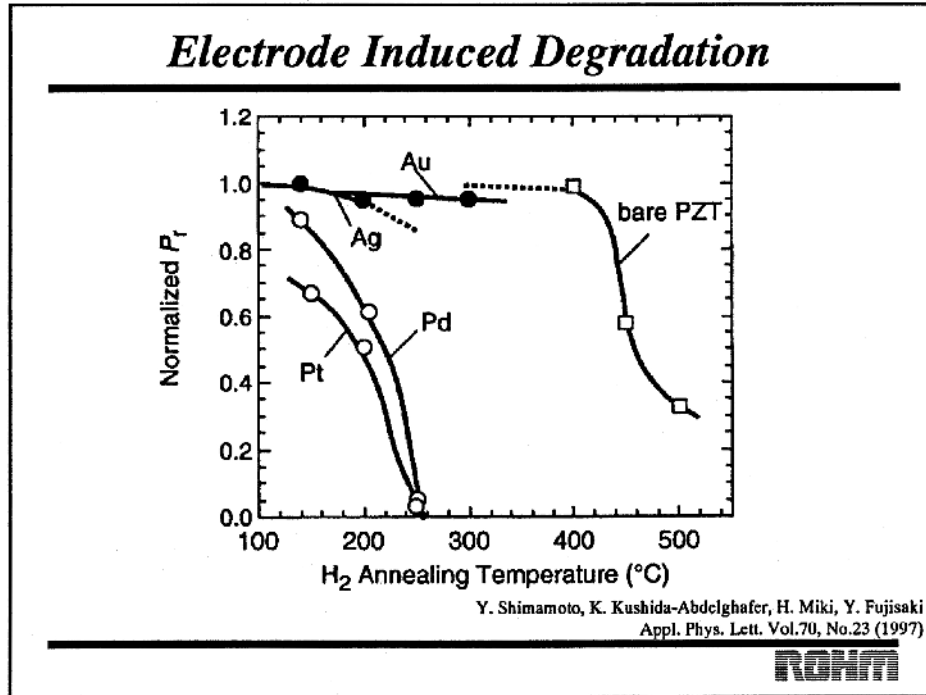

Fig. 8. Electrode induced degradation.

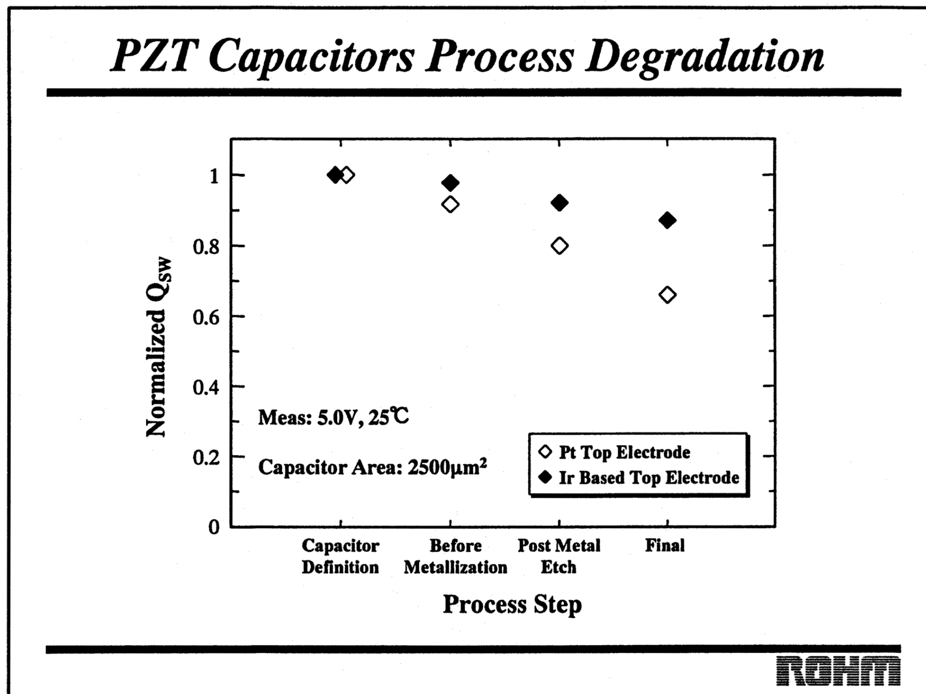

Fig. 9. PZT capacitors process degradation.

Reliability Test Results

Test Item		LOT A	LOT B	LOT C	LOT B'	LOT C'
		PNG/N	PNG/N	PNG/N	PNG/N	PNG/N
	240h	0/30	0/30	0/30	–	–
B/IN	500h	0/30	0/30	0/30	–	–
(125C)	1000h	0/30	0/30	0/30	–	–
PCT	300h	0/30	0/30	0/30	–	–
(121C,100%)	500h	0/30	0/30	0/30	–	–
TCY	300cyc	0/30	0/30	0/30	–	–
(150C/-65C)	500cyc	0/30	0/30	0/30	–	–
	240h	0/30	0/30	0/30	–	–
HST	500h	0/30	0/30	0/30	–	–
(150C)	1000h	0/30	0/30	0/30	–	–
HAST	200h	0/30	0/30	0/30	–	–
(130C/85%)	300h	0/30	0/30	0/30	–	–
	240h	0/100	0/100	0/100	0/99	0/100
Retention	500h	0/100	0/100	0/100	0/99	0/100
(150C)	1000h	0/100	0/100	0/100	0/99	0/100
Fatigue	1E+09cyc	0/100	0/100	0/100	–	–
Ret after Fatigue	1E9&1000h	0/100	0/100	0/100	–	–

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Fig. 10. The results of reliability test of ferroelectric memory chips.

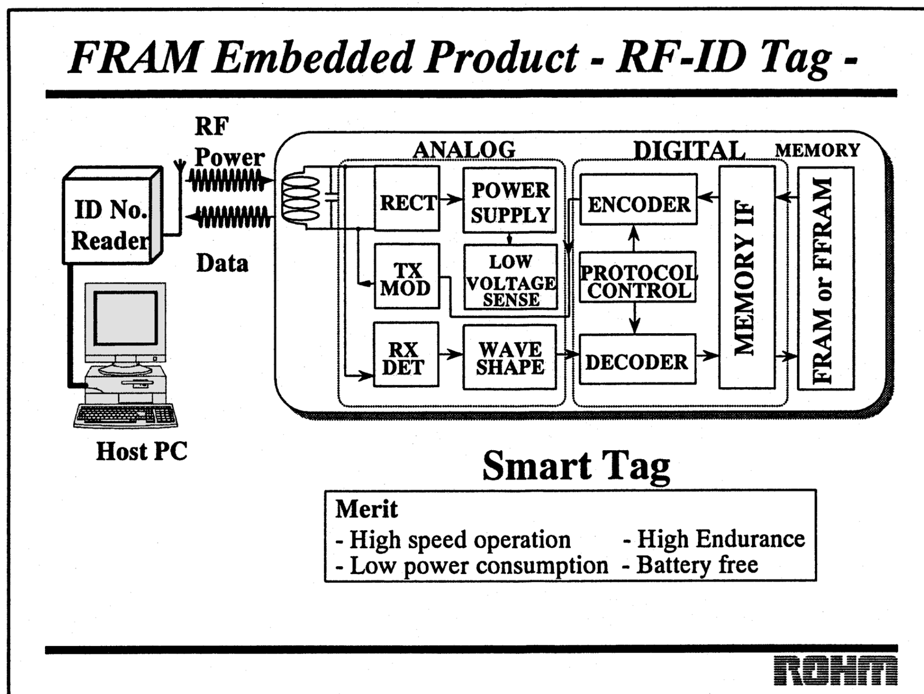

Fig. 11. FRAM embedded product RF-ID tag.

FLASH memory is embedded in the CMOS logic/analog device, original CMOS designed cell libraries are not applicable. The Ferroelectric memory embedded approach is most suitable from the process viewpoint and CMOS cell libraries are able to used without modification.

Fram Embedded Application

The features of ferroelectric memories are not only replacing the existing memory market, but also creating new application fields, and are impacting society.

As the importance of ecology is increasing, ferroelectric memories will be getting more important. For example, battery back SRAM will be replaced by ferroelectric memories, because of the disposal of used batteries. A ferroelectric memory has more advantages as a memory embedded product than other conventional memories, because of its non-volatile, high speed writing/programming, low power supply voltage, high endurance and good CMOS process adaptability. Ferroelectric memory embedded RF-ID tag/contactless smart IC cards are one of the most adequate examples.

They require power as low as possible, because they get power from RF without having a back up battery as shown in Figs. 11 and 12.

RF-ID tags/contactless smart IC cards will change our life style in various fields. Some trials or investigations are being carried out in the following applications; logistics control, medical care, bank card/electronic purse, airline bag tags, pre-paid cards, courier, postage, passport, license cards and ID cards etc.

A courier system is under progress to be combined with a logistics system, both systems have a strong demand for use of RF-ID tags or contactless IC cards for automatic sorting, and logistic data transmissions between an ID card and a read/program terminal keeping some remote distance.

RF-ID cards are not only used for identification but for data storage and data transmission, and enable the connection of a courier information and logistic information in the same network.

1.9 billion of parcels were handled including 0.5 billion postal parcels in 1995 in Japan, this volume is

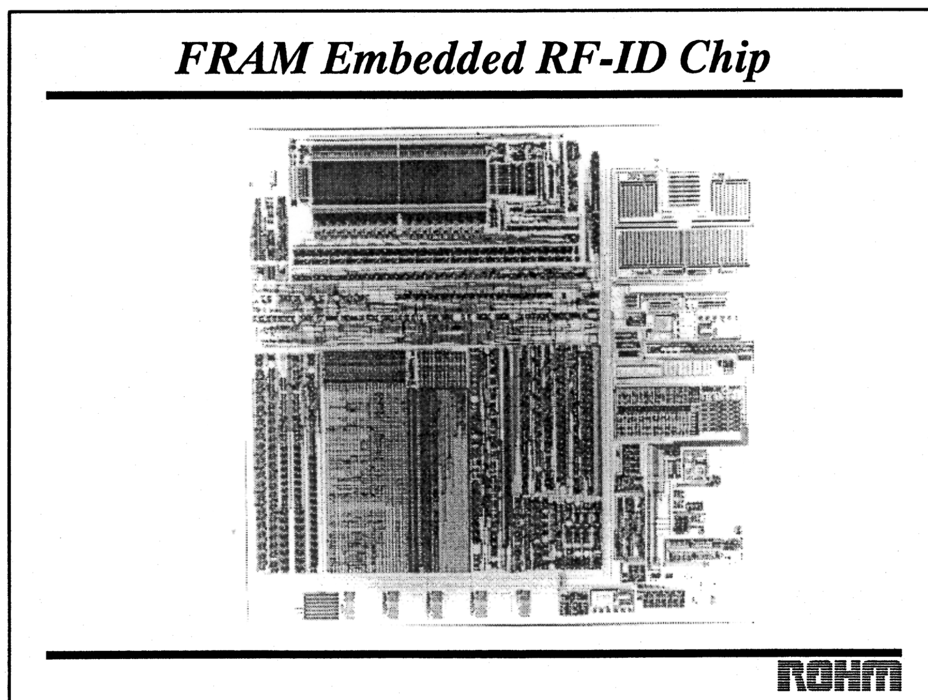

Fig. 12. FRAM embedded RF-ID IC chip.

growing 10% at annual base. The demand for RF-ID cards becomes more important with the increase of the customer's variety of requirements such as many kinds of parcels with a small volume of each type, reduced delivery time, frequent delivery with a small lot, mistake and cost reduction. The demand for RF-ID cards is expected to be up to 10–20 billion cards per year.

Recently, flash memory embedded system LSI chips are being popular, especially flash memory embedded CPUs are used in many electronic systems. A simultaneous multi-process implementation of fine electronic control is required in recent systems. As performance of software algorithms give more influence to a system, development of algorithms takes more time. Under these circumstances, conventional mask ROM embedded type CPUs have a more difficult task for achieving a short development cycle, give the revised LSI have to be made again to change the ROM when the software has a bug.

If mask ROM is replaced to flash memory, LSI is able to be manufactured without a waiting completion of software development. An algorithm installation in a CPU should be done after fab out set by writing the program to the flash memory embedded to a LSI chip.

In addition, flash embedded architecture enables one to upgrade the software without changing the LSI chip.

Further, if FRAM is applied as embedded ROM and RAM for CPU, in system programming becomes reality.

It is not far away to change software or to have learning function and takes the learning results in the system to change a configuration of a system.

A New Device Architecture

Ferroelectric memories have many advantages in standard memory applications as described above, as well as applications to RF-ID cards with ferroelectric memories creating more advantages than using conventional non-volatile memories.

Today, the integration level of ULSI is getting extremely high, up to several million transistors on a

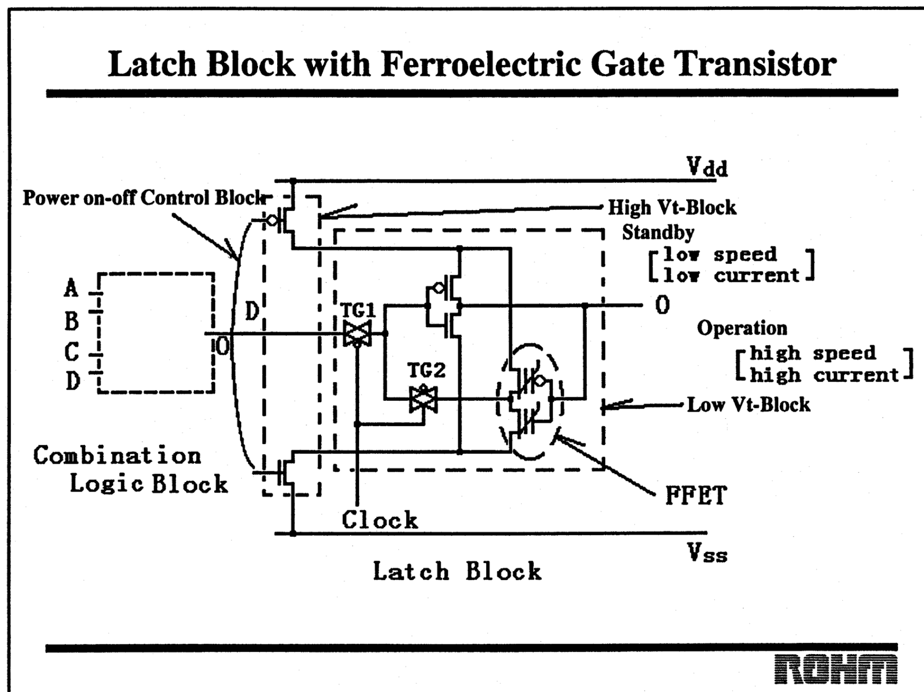

Fig. 13. Latch block with ferroelectric gate transistors.

chip, and by the year 2010 one billion transistors will be integrated.

Such a super high-integrated chip will never be produced economically without having any redundant circuits in it.

But this problem will be solved by the FPGA approach, because a redundancy function is easily introduced in FRAM. The ferroelectric memory technology enables the use of a smaller switch memory cell to be compared to conventional SRAM based FPGA, and no back-up memory is required with ferroelectric memory based FPGA.

The small cell of FPGA with the ferroelectric memory will spread to more than 500 K gate count of FPGA with fine cell architecture similar to gate array.

This ferroelectric memory based FPGA can have a good security function to protect from having the circuit copied. Further, a more important feature of this FPGA is that it will take self-learning results into the logic circuit configuration during operation in a system, because of its high speed programming and no additional high voltage power supplied requirement on board. This ferroelectric memory FPGA can be used as Dynamic Programmed Gate Array (DPGA), and in system programming of hardware VIA telecommunication line will become available by using DPGA technology. This DPGA will open the new world for the system hard ware, which will be reconfigured instantly by request.

Instead of using dual threshold transistors, ferroelectric gated transistors or ferroelectric capacitors can be used to minimize the electric power consumption and the number of transistors used in logic circuits as shown in the Figs. 13 and 14. The latch circuit used in ferroelectric gated transistors or ferroelectric capacitors can keep the logic status even when the electrical power is lost. The previous latched data will be given when electrical power is supplied back to the circuit. By applying this method in a large logic circuit, the electrical power supply is not required for low power application, just for keeping the logic status, and a local power off (no electrical power supply on some area of large logic circuit) approach will takes position.

Ferroelectric memories have a good match well to the conventional CMOS devices, existing cell library portfolios can be utilized in ferroelectric memory embedded products as shown in Fig. 15.

The ferroelectric memory technology will lead to new semiconductor device architecture, including a neuron device using ferroelectric memories as analog memory, and will take the major place in the coming multi-media era.

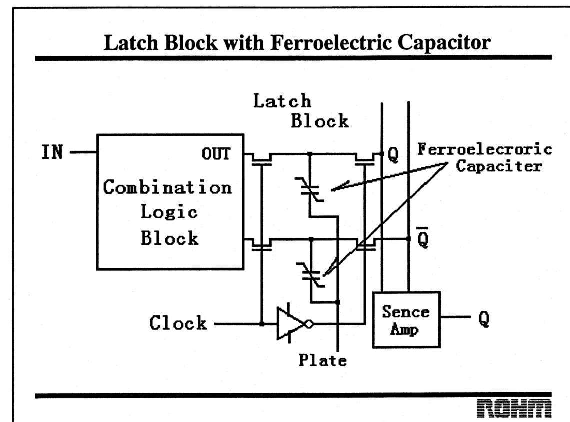

Fig. 14. Latch block with ferroelectric capacitors.

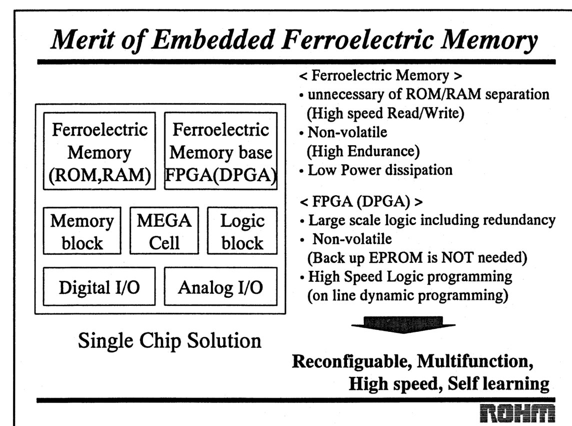

Fig. 15. Merit of embedded ferroelectric memory.

Conclusion

The ferroelectric memory technology will have a big impact on the existing semiconductor memories, and open new application fields, which will change our life style, on enable new device architectures for the 21st century.

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